What is claimed is:

1. A semiconductor memory device, comprising:

a cell area having N+1 number of unit cell blocks, each including M number of word lines;

a predetermined cell block table for storing a candidate information representing at least more than one candidate word line among the M number of the word lines to be stored data; and

a tag block for receiving a row address, sensing a logical cell block address in the row address and outputting a physical cell block address based on the logical cell block address and the candidate information,

wherein the tag block includes:

a N+1 number of unit tag tables, each having M number of registers and storing a store information that the registers corresponds to M number of word lines, each register storing each the physical unit cell block address in response to the logical cell block among unit cell block addresses having a word line in response to the candidate information; and

an initialization unit for initializing the N+1 number of unit tag tables.

2. The semiconductor memory device, further comprising:

a control means for controlling the tag block and the predetermined cell block table for activating one word line of a unit cell block selected by the physical cell block address.

3. The semiconductor memory device as recited in claim 1, wherein the initialization unit includes:

a plurality of logical OR gates for respectively receiving an initialization selection signal to initialize the N+1 number of unit tag tables and tag table selection signal to select one of the N+1 number of unit tag tables and respectively outputting each of initialization activating signals to each of the N+1 number of unit tag tables;

a plurality of first multiplexers controlled by the initialization selection signal for selectively outputting one between the input logical cell block address and each of initialization signals to initialize each of the N+1 number of unit tag tables to each of the N+1 number of unit tag tables; and

a plurality of second multiplexers controlled by the initialization selection signal for selectively outputting one between a local address to select M number of word lines included in each of the N+1 number of unit cell blocks and an initialization address to select all register included in one of the unit tag table.

4. A method for controlling a tag block for assigning a physical unit cell address based on a logical unit cell block, comprising the steps of:

a) initializing the tag block in a semiconductor memory device; and

b) performing a normal operation of the semiconductor

memory device by using the tag block.

5. The method as recited in claim 4, wherein the step a) includes the steps of:

a-1) nullifying the N+1 number of unit tag tables;

a-2) selecting the N+1 number of unit tag tables; and

a-3) storing each different logical unit cell block information in the N number of unit tag tables among the N+1 number of unit tag tables.